Theory and Applications of the Si7660 and Si7661 Voltage Converters

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Introduction

Many times a simple digital circuit design can be greatly complicated by the needs of just one or two of the on-board devices. For example, analog devices often used along with digital circuits (such as op amps and data acquisition systems) are notorious for negative voltage requirements of −5, −10 or −15 V when everything else in the circuit needs only positive voltages. Until recently, the only answer was to either buy a dc-to-dc converter module (expensive) or redesign the power supply to generate the negative voltages (expensive and wasteful in parts count and space). This application note presents the best alternative to this problem: the Si7660 and Si7661 monolithic voltage converters. With the Si7660 and Si7661, negative voltages from 1.5 to 20 V can be generated from a positive supply with minimum parts count and minimum cost.

Theory of Operation

The basic theory behind the Si7660 and Si7661 is the same and is based on the ideal voltage doubler shown in Figure 1. Capacitor C_1 is the pump capacitor, and C_2 is the reservoir capacitor. The pairs of switches (S_1 with S_3, and S_2 with S_4) are driven by an oscillator/toggle circuit, providing charge and transfer cycles of equal length.

During the charge cycle, S_1 and S_3 are closed, and current flows into C_1, charging it to the value of V_{IN}. The oscillator toggle then changes state, and the transfer cycle begins. S_1 and S_3 are opened while S_2 and S_4 are closed, allowing C_1 to dump charge into C_2 until the potential across them has equalized. The oscillator/toggle then switches again, and the process starts over.

For no load conditions, the voltage inversion will be virtually perfect since the amount of charge that must be transferred from C_1 to C_2 will be limited to losses due to leakage from C_2 and any parasitic capacitances. As the load increases, C_1 must transfer more and more charge to make up for the depletion of C_2 as it supplies current to the output during the charge cycle. This action causes the output voltage to drop, making the circuit appear to be a perfect inverter in series with an output resistor that varies in magnitude with the input voltage. Figure 2 shows this concept in a two port diagram of the device, and Figure 3 illustrates the typical output characteristics of both devices configured in the inverter mode.

Circuit Operation

With the Si7660 and Si7661, the only parts of the doubler not included inside the package are the pump and reservoir capacitors. The internal switches are made with p-channel and n-channel MOSFETs. The main difference between the Si7660 and Si7661 is the breakdown voltage of the MOSFETs which in turn dictates the maximum input voltage. Also, the design of the Si7661 offers a much greater resistance to device latchup, which is discussed later. Since the internal sections of the two devices are very similar, description of the operation of the Si7660 and Si7661 is combined. The internal sections of the circuit are the oscillator, divider, regulator, level translator, and substrate logic. Figure 4 shows a block diagram of the internal sections of the inverter circuit.

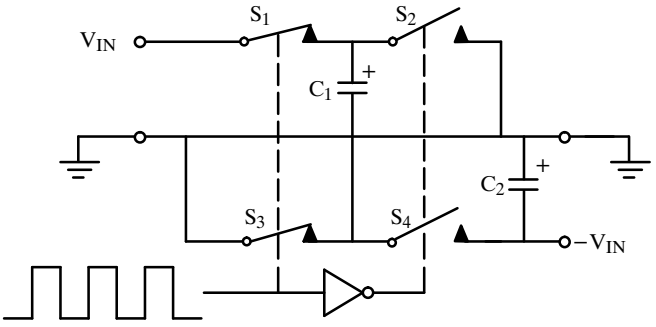


Figure 1. The Ideal Voltage Doubler

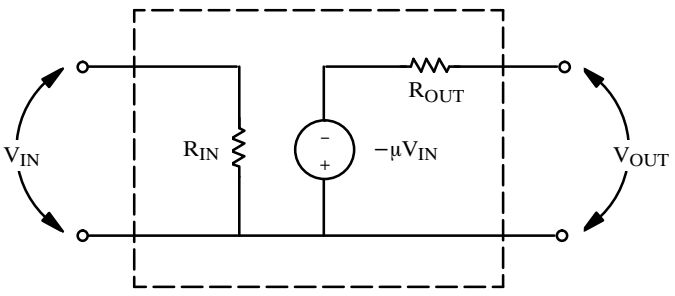
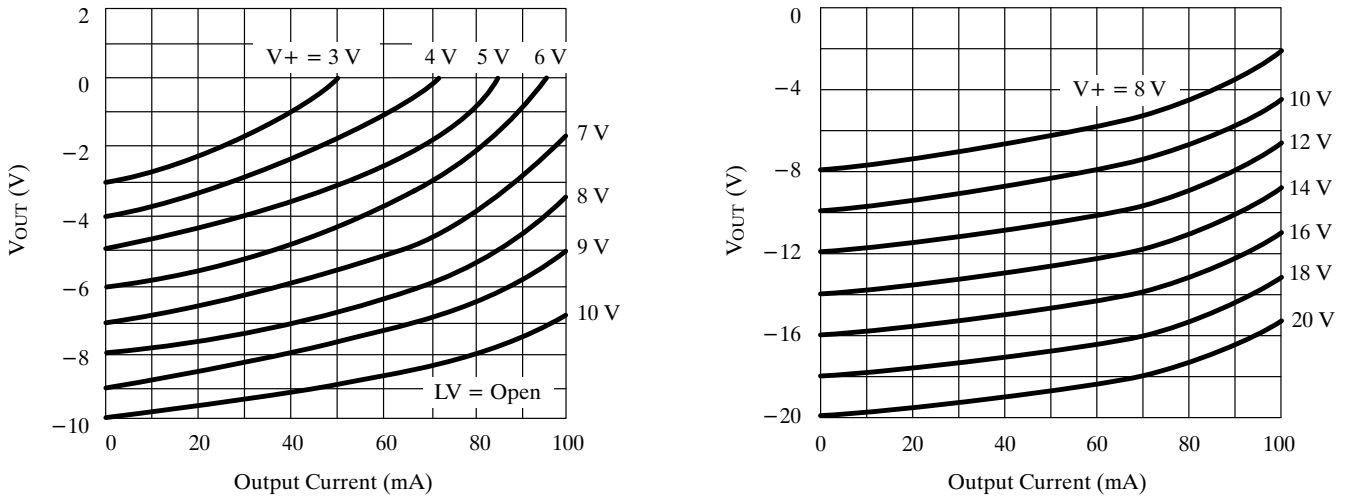


Figure 2. Two-Port Diagram of the Voltage Converter Circuit



(a) Output Characteristics of the Si7660 Voltage Converter

(b) Output Characteristics of the Si7661 Voltage Converter

Figure 3.

The oscillator supplies the signal to the divider section which in turn drives the rest of the circuit. The OSC input has an input impedance of approximately 1 mΩ. This allows the internal oscillator to be overridden by an external clock or to be slowed down by the addition of an external capacitor.

The internal regulator is a series voltage regulator with a zener reference to insure that low voltage components of the circuit are provided with no more than 5 V when the input voltage is greater than 5 V. It also provides current limiting for the oscillator and divider circuits. When the input voltage is less than 3.5 V for the Si7660 (less than 9 V for the Si7661), the LV pin is grounded, bypassing the internal regulator. However, when the Si7660 is operated above 3.5 V, the LV pin must be left open to provide latchup protection. For the Si7661, LV should be left open above 9 V for proper operation.

The divide-by-two counter provides complementary outputs. Q and $\overline{Q}$ drive the inputs of the level translators, which in turn provide the necessary switching voltages to drive the MOSFET switches. The built-in delay of the translators guarantees that break-before-make action occurs.

The substrate logic network insures that two things happen. First, it makes sure that the substrate-source/drain junctions of Q_3 and Q_4 are never forward biased, and that the on-resistance of each of the output transistors will be as low as possible for all operating conditions. Second, the network determines the most negative voltage in the device and uses it to supply power to the level translator.

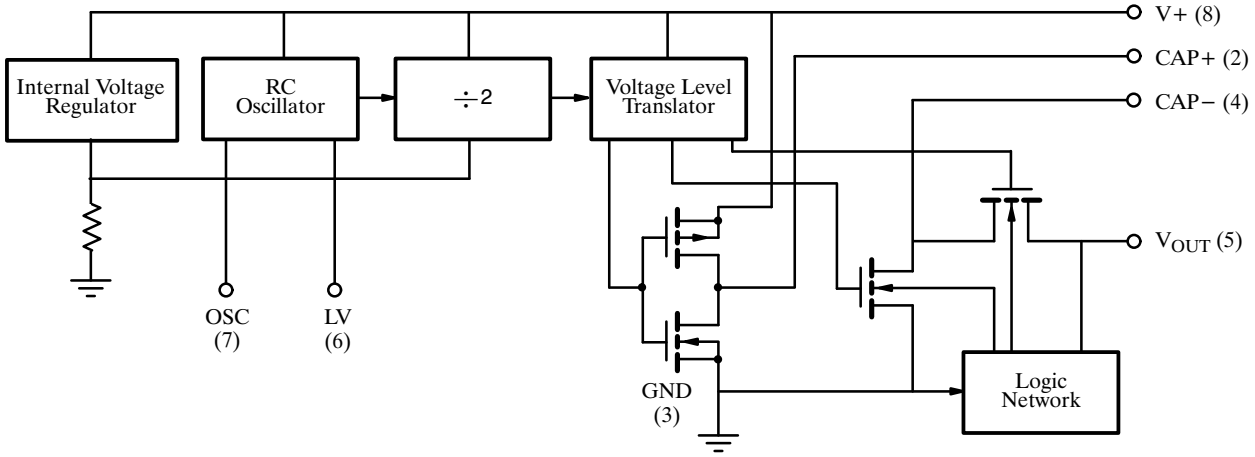


Figure 4. Block Diagram of the Voltage Converter Circuit

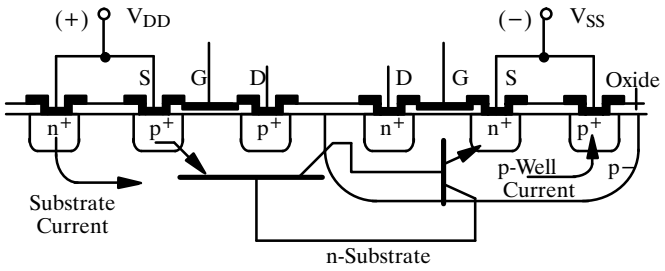


Figure 5. Intrinsic SCR Superimposed on a CMOS Gate Structure

Latchup

Because of the basic internal four-layer geometry of CMOS devices, an intrinsic SCR exists. Figure 5 depicts the SCR structure. The source of the n-channel device becomes the SCR cathode; the source of the p-channel is the anode; and either drain can act as a gate. Since an SCR does not trigger until certain conditions occur, it can sometimes cause no problems at all, yet sometimes it may be fatal to a CMOS device.

The intrinsic SCR needs three conditions to cause latchup: the betas of the two parasitic transistors must be greater than one; the current flowing through the channels of the devices must be greater than the holding current of the SCR; a pulse must be applied to one of the gates to trigger the SCR action.

The trigger can come from several sources: the power-up sequence may cause problems if the SCR gate receives power before the other terminals. Another possible trigger source is a high slew rate across the intrinsic SCR. When the SCR is triggered, the CMOS devices are suddenly shorted out, and the output impedance of the device becomes very low.

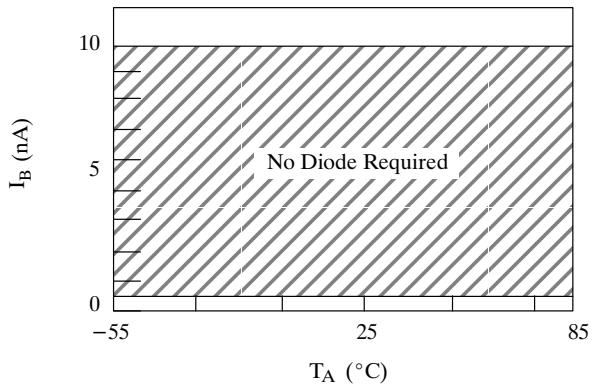


Figure 6. Range of Input Voltage and Operating Temperature for the Si7660

To prevent damage to older versions of the Si7660 when conditions for latchup occured, a diode was used in serieswith the V_{OUT} pin to block the discharge of C_2 and keep the current below the holding value of the SCR. This diode was used whenever the input voltage could exceed 6.5 V at room temperature. Figure 6 shows the operating range of the improved Si7660.

The Si7661 is a higher voltage device than the Si7660, and is designed on a different process. This high voltage silicon gate process reduces the parasitic betas in Q_4 to a value that makes it extremely difficult to produce the conditions for latchup. Because of this, the series diode is not needed for proper operation.

General Applications

The Si7660 and Si7661 are mainly intended for use as voltage inverters. However, with a few added components, the inverter circuit can be rearranged to provide many different voltage levels. In some configurations, they can even provide more than one voltage output at the same time. The possibilities include voltage inversion, voltage multiplication, and even simultaneous inversion and multiplication.

Basic Voltage Inversion

With no load, the output voltage magnitude of the basic voltage inverter circuit shown in Figure 7 will typically be within 0.1% of the V+ (input voltage) magnitude for the Si7660 and within 0.3% of the input voltage magnitude for the Si7661. As the load current increases, the output will drop as shown in Figure 8 (a). The effective output resistance will vary with input voltage as given in Figure 8 (b). Once the load current reaches its limit (30-40 mA for the 5-V case), the inverter can no longer regulate the voltage properly and shuts down to protect itself from extreme power dissipation.

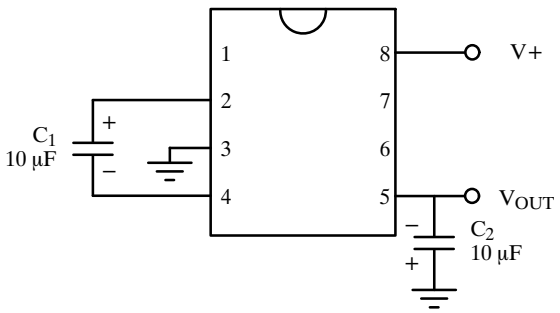
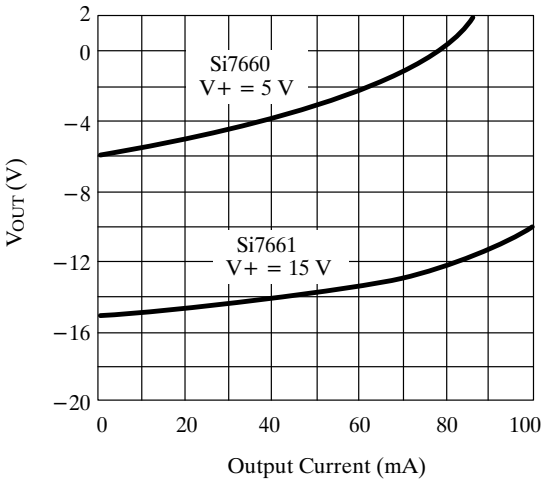
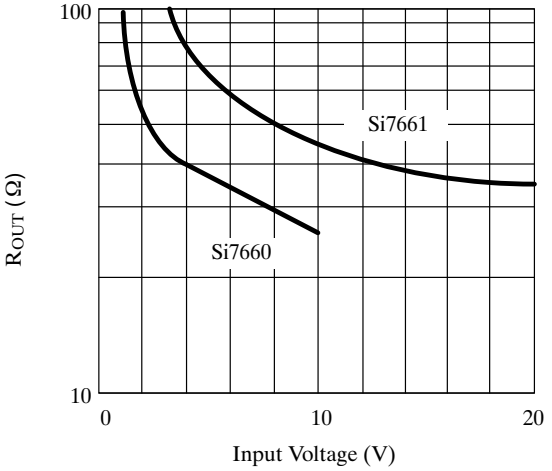


Figure 7. Schematic Diagram of the Basic Inverter Circuit



(a) Variation of Output Voltage as a Function of Output Current



(b) Variation of Output Resistance as a Function of Input Voltage

Figure 8.

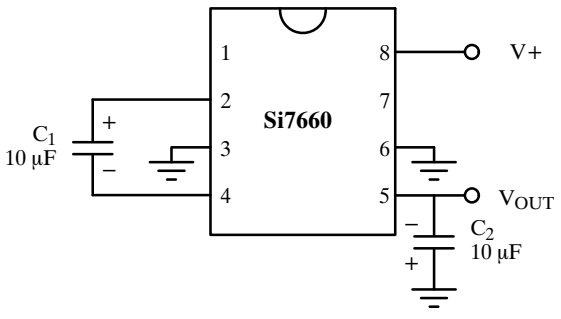


Figure 9. Inverter Circuit Connections for Low Voltage Operation

Table 1. Effect of Varying the Pump and Reservoir Capacitor Size on Output Ripple Noise

	Capacitors (µF)	V_{OUT} (V)	VR (mV_{P-P})
Si7660	10	−3.838	150
Inverter Mode	22	−3.862	75
(See Figure 7)	47	−3.873	30
V+ = +5 V	100	−3.874	26
I_{OUT} = 10 mA	470	−3.879	10
	1000	−3.880	5
Si7661	10	−13.849	175
Inverter Mode	22	−13.872	80
(See Figure 7)	47	−13.882	38
V+ = +15 V	100	−13.883	29
I_{OUT} = 10 mA	470	−13.885	10
	1000	−13.890	5

CAUTION: At higher input voltages (for either device), the output maximum limit can cause the power dissipation to exceed the maximum rating of the package (especially plastic). Always calculate the maximum power dissipation for your design.

The output ripple of the inverter is a function of the oscillator frequency as well as the size of the pump and reservoir capacitors. The nominal oscillator frequency is 12 kHz for the Si7660 and 10 kHz for the Si7661. Because the output ripple is important in some linear applications where supply noise is critical, Table 1 provides ripple values for different pump and reservoir capacitor values.

It is important to note that increasing the capacitor size can lead to other difficulties. The main problem is that the large capacitors may draw excessive amounts of current at turn-on. If the current is too great, the power dissipation of the device can be exceeded causing destruction of the converter. Even when the device is running, the charge transfer under heavy loads can push the switches to their limits.

As stated before, the LV pin shorts out the internal regulator at low voltages when it is tied to ground. The LV pin should be grounded for operation below 3.5 V for the Si7660 and 9 V for the Si7661. However, it is necessary to leave the LV pin floating for high voltage operation, as shown in Figure 7. Failure to do so could permanently damage the device. Figure NO TAG shows the inverter configured for low voltage operation.

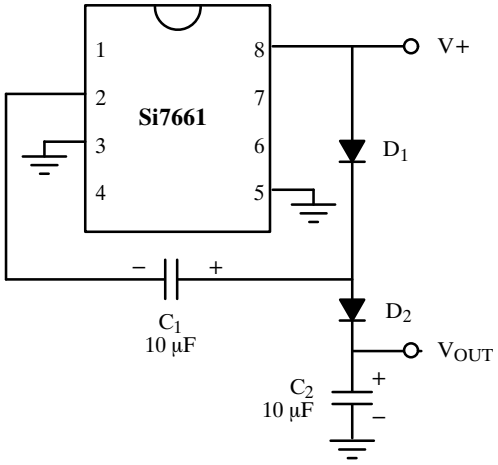


Figure 10. Voltage Doubler Schematic Diagram

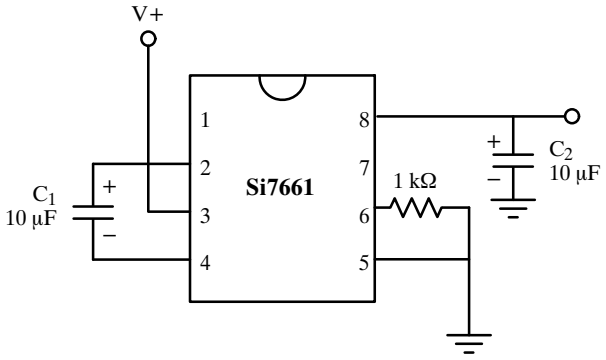


Figure 11. Alternate Voltage Doubler Schematic Diagram (for use with Si7661 only)

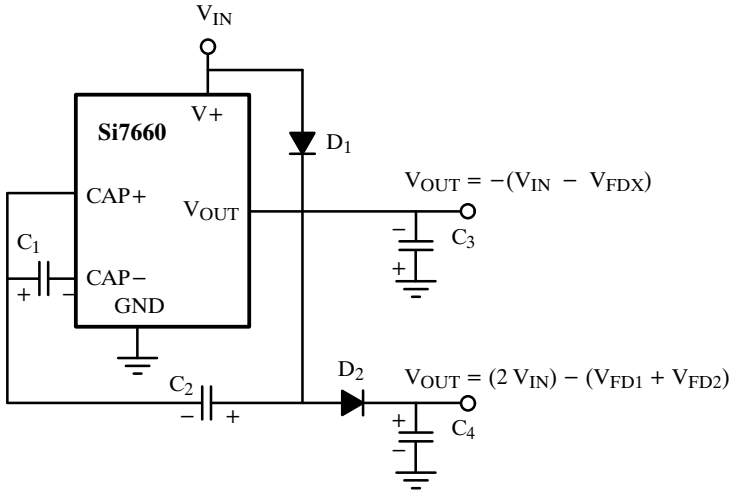


Figure 12. Combination Inverter/Multiplier Circuit

Voltage Multiplication

Figure 10 gives the schematic diagram of the voltage doubler. This circuit requires only two additional diodes and will provide positive voltage multiplication at the expense of the voltage drops of the two diodes in series with the output. This means the positive multiplier will not be able to provide the near perfect output function like the basic inverter circuit does. The output voltage of the multiplier will be:

$$V_{OUT} = 2\,(V+) - 2\,V_{diode} \quad (1)$$

The circuit of Figure 10 can also be used as a negative-to-positive voltage converter. To do so, set Pin 8 to Ground and Pins 3 and 5 to the negative input voltage, V−. The output voltage will then be:

$$V_{OUT} = |\,V-\,| - 2\,V_{diode} \quad (2)$$

Another doubler circuit can be built with the Si7661 that will eliminate the diode drops and give a much more efficient output voltage. Figure 11 illustrates this circuit which takes advantage of the bi-directionality of the CMOS output transistors. The 1-kΩ resistor injects a current into the LV pin to insure that the oscillator starts. **Note: This circuit cannot be used for the Si7660 due to oscillator protection circuitry inherent to the circuit.**

Simultaneous Inversion and Multiplication

The circuit shown in Figure 12 will provide both positive multiplication and inversion at the same time. The output voltages will be the same as those given in equations 1 and 2. This configuration is limited by the load current that can be drawn out of either output before the circuit becomes overloaded.

Parallel Connection

Although a single Si7660 and Si7661 cannot supply very large amounts of current, higher currents can be provided when several devices are connected in parallel. As shown in Figure 13, two or more inverter circuits can be paralleled to provide a lower output resistance, providing a smaller output voltage drop for a given current. This circuit will also expand the operating output current ranges slightly. Each device must have its own pump capacitor, but the reservoir capacitor is shared between all of the devices.

When two or more devices are paralleled, the output noise (ripple) will contain not only components at frequencies of each of the oscillators, but also at sum and difference frequencies due to a mixing action at the inverter outputs.

If such noise cannot be tolerated, the OSC pin of one of the devices can be driven by an exclusive NOR gate that compares the oscillator frequencies of the two devices as shown in Figure 14. This forces the two devices to alternate their charge and transfer cycles, which will not only reduce output noise but also maximize efficiency.

Series Connection

When high voltage inversion is desired, inverter circuits can be placed in series to produce voltage outside of the operating range of a single Si7660 or Si7661. Figure 15 shows two inverters cascaded to double the input voltage magnitude while inverting the voltage at the same time.

When cascading devices, however, the power dissipation of each device must be considered. As each new stage is added, the previous stages will be subjected to more and more load current, from both the quiescent current of the new stage and the multiplying action of the load current through each of the stages, as shown in Figure 16.

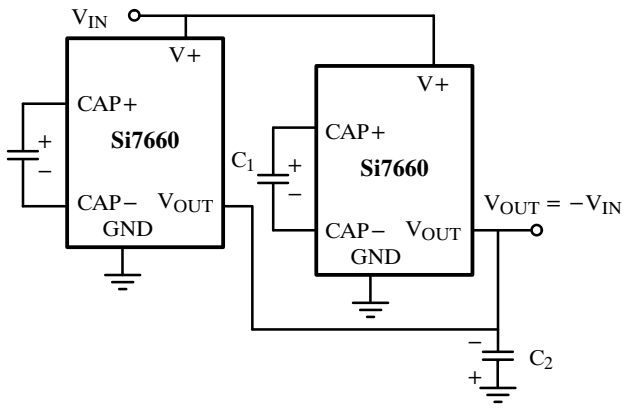


Figure 13. Paralleling Multiple Voltage Converters for Increased Current Capability

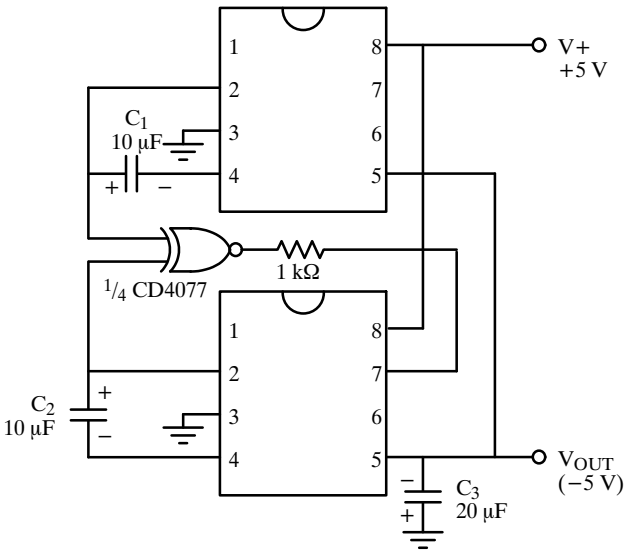


Figure 14. Synchronizing Two Si7660s or Si7661s With a Single Exclusive NOR Gate

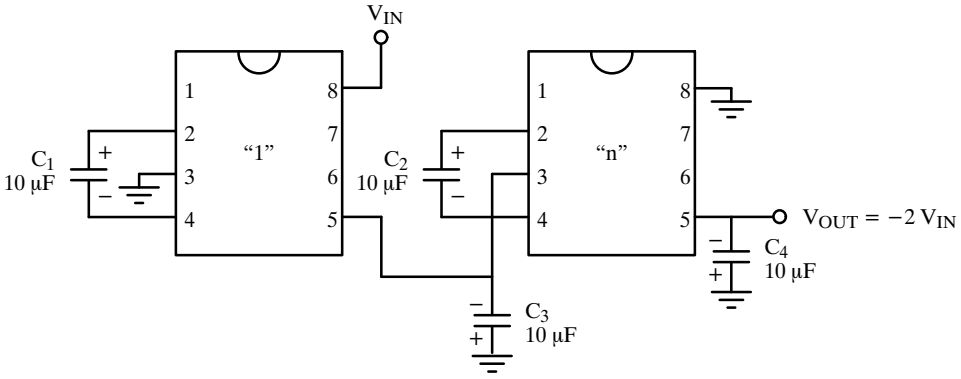
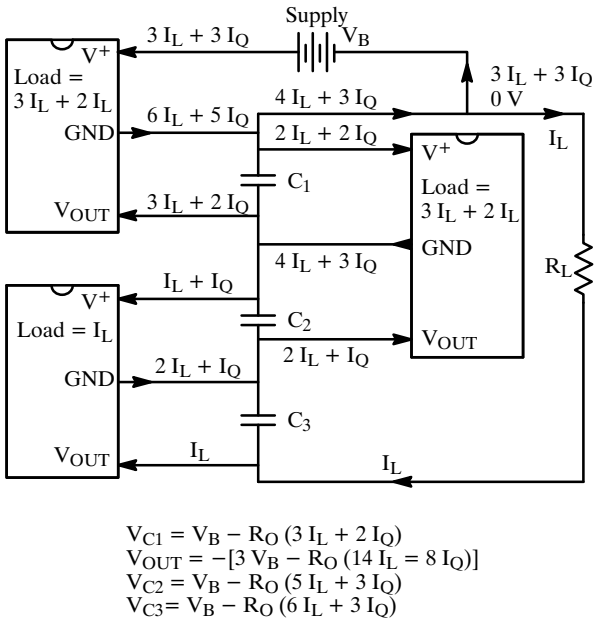


Figure 15. Cascading Devices For Greater Output Voltage Range



$V_{C1} = V_B - R_O (3 I_L + 2 I_Q)$
$V_{OUT} = -[3 V_B - R_O (14 I_L = 8 I_Q)]$
$V_{C2} = V_B - R_O (5 I_L + 3 I_Q)$
$V_{C3} = V_B - R_O (6 I_L + 3 I_Q)$

Figure 16. Current Model of Cascaded Voltage Converters

As the number of cascaded devices increases, the effective output resistance also increases which will severely reduce the output voltage for a given current level when compared to a single inverter. This effect can be reduced by paralleling devices in the first stages, though the cost in parts increases twofold for every added stage.

Changing the Oscillator Frequency

The typical oscillator frequencies were given in the description of the basic inverter circuit.

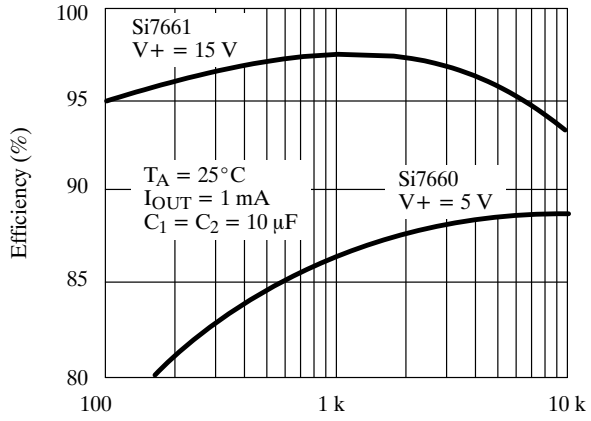
However, Figure 17 (a) shows that the maximum power efficiency is not achieved at the typical oscillator frequency. If maximum power efficiency is desired, an external capacitor can be connected between the OSC pin and ground. Figure 17 (b) illustrates the effect of added capacitance on the oscillator frequency. A resistor connected from the OSC pin to V+ may be used to increase the oscillator frequency. This will reduce ripple amplitude at the expense of reduced efficiency. Values above 2 MΩ are usually adequate.

If synchronization with an external driver or clock is needed, the OSC pin can be driven either by a TTL or CMOS logic gate. Figure 18 provides the proper circuits for interfacing to either logic standard. Note that the TTL interface can only be directly connected to the OSC pin if the circuit is using a 5 V supply. If the input voltage is other than 5 V, some type of buffer circuit will be required. The charge/transfer transitions will occur on each rising edge of the clock.

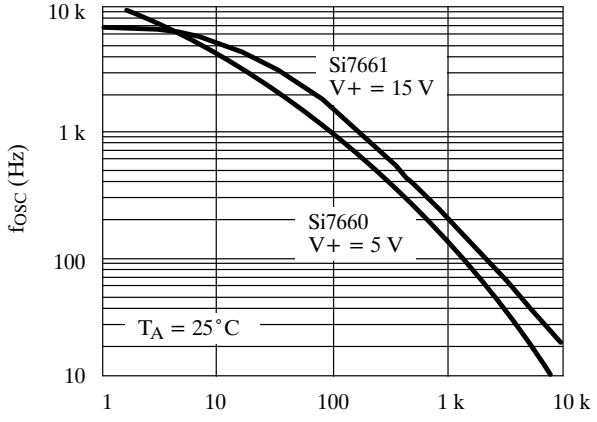
Specific Applications

When looking at possible applications for the Si7660 and Si7661, it must be remembered that these devices are VOLTAGE sources, not CURRENT sources. Therefore, any heavy load will either greatly reduce output voltage (possibly out of the desired range) or cause the device to go into power shutdown. If the concept of VOLTAGE conversion is kept in mind, many problems will be avoided.

There are many places where a low current negative supply made with an Si7660 or Si7661 would do just as well as a full conventional negative supply or dc-to-dc converter module.

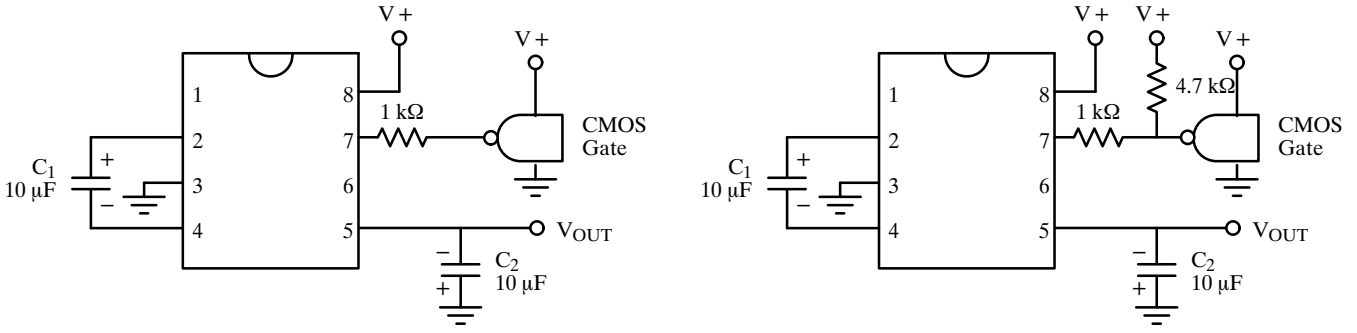


(a) Graph of Efficiency vs. Oscillator Frequency



(b) Graph of Oscillator Frequency vs. Added Capacitance

Figure 17.



(a) CMOS Drive Circuit for the Si7660 or Si7661

(b) TTL Drive Circuit for the Si7660 or Si7661 (5-V input only)

Figure 18.

Some examples of possible uses are power sources for operational amplifiers, dynamic RAM's, microprocessors, and data conversion products. Several examples of these systems are given below.

Memories

Several different memory manufacturers produce 16 K x 1 dynamic RAM's that have a need for a −5-V low current supply to provide substrate biasing. The National MM5290, AMD AM9016, and THOMSON MK4116 all use this type of arrangement. Table 2 gives the −5-V supply current requirements for each of these devices.

The only constraint in using the Si7660 or Si7661 for this application is when calculating the voltage fluctuations that will occur when a location is read from or written to. Make sure that the ABSOLUTE MAXIMUM current is considered so that the negative supply for the dynamic RAM will not be pulled down more than 5% (below 4.75 V) during a memory read or write. Even with the maximum current taken into account, the Si7660 or Si7661 could easily provide the negative supply voltage supply for an entire 16 K x 8 dynamic memory bank.

Table 2.
Current Requirements of Several Different Dynamic RAMs

Device	Operating Current (µA)	Standby Current (µA)	Refresh Current (µA)
MM5290 (0 to 70°C)	200	100	200
AM9016 (0 to 70°C)	200	100	200
AM9016 (−55 to 85°C)	400	200	400
MK4116 (0 to 70°C)	200	100	200

Op Amps

Operational amplifiers are one of the most commonly used integrated circuits and often use negative supply voltages. Although some op amps can supply high current loads, more often the current requirements involved are well within the capabilities of the Si7661.

Figure 19 shows the Si7661 supplying the negative voltage to a 741 op amp configured as an inverting amplifier. As the current drain through the negative supply terminal of the op amp increases, the output voltage of the Si7661 will decrease. However, this will not affect the output capability of the op amp at its rated output current.

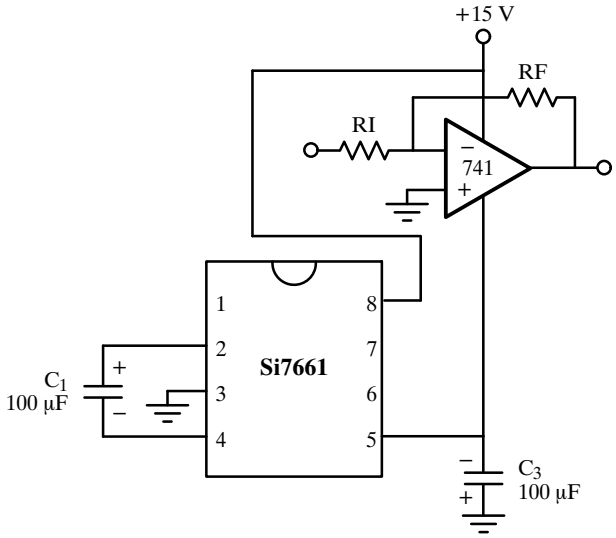


Figure 19. Using the Si7661 to Generate the Negative Rail for a 741 Op Amp

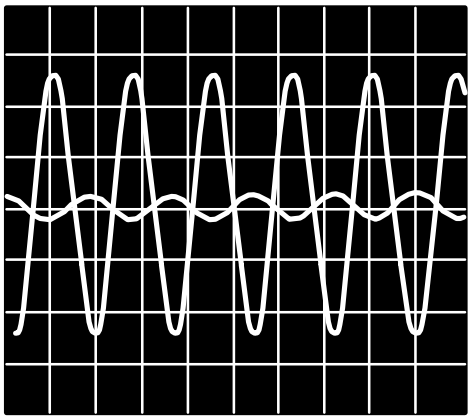


Figure 20. Input and Output of the 741 Inverting Amplifier at Maximum Undistorted Output

Figure 21 illustrates this with a photograph of the input and output of the circuit in Figure 19 when a 1 kΩ load was placed on the amplifier output. The output was undistorted to 26 V peak-to-peak.

The output ripple of the Si7661 must be taken into consideration when using it as an op amp supply. Some op amps do not have adequate power supply rejection to withstand the ripple noise level of the Si7661. The pump and reservoir capacitors can be chosen to minimize this noise condition (see Table 1). The ripple should be measured at the maximum negative supply current (i.e., rated load) to determine if the Si7661 can be used to supply the op amp.

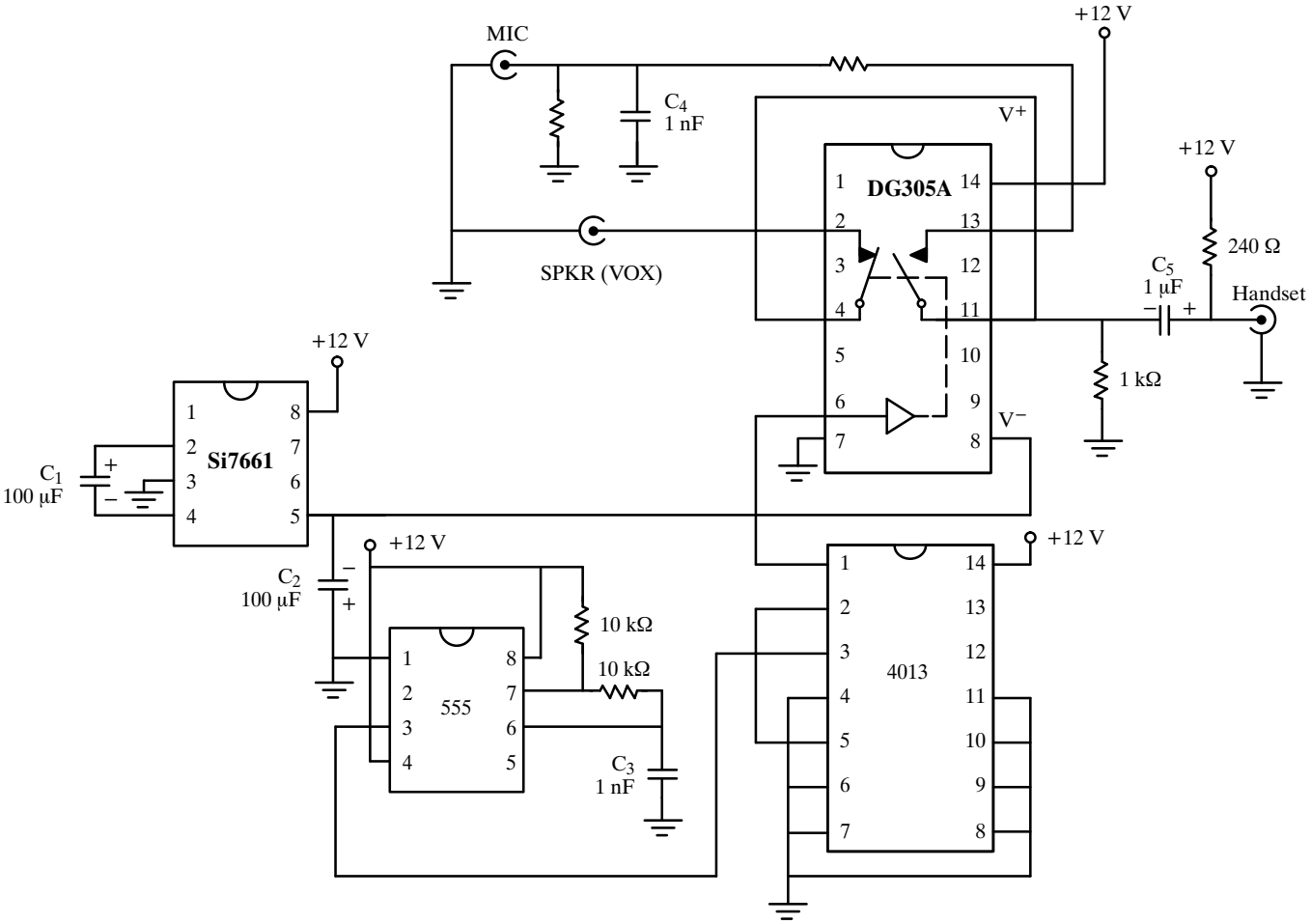


Figure 21. Using the Si7661 to Supply a Low-Current Analog Switch

Analog Switches

Figure 21 gives the schematic diagram of a circuit that was used to interface a Northern Telecom telephone set to an ICOM 2AT2-meter amateur radio transceiver.

The analog switch provides isolation for the microphone and speaker connections of the transceiver since the telephone set uses a single path for both transmission and reception. The telephone was operated at 12 V for direct interface to the DG305A, and the supply current from the Si7661 was < 1 mA.

Microprocessors

Some of the older standard microprocessors need a negative supply for substrate biasing. The Intel 8080 microprocessor is a good example of this. It is an inexpensive 8-bit CPU that has many different support chips available. To provide the negative supply voltage (-5 V), a basic inverter circuit (such as in Figure 7) using an Si7660 is connected to Pin 11 of the microprocessor. The 8080 negative supply draws a maximum current of 1 mA which will not pull down the supply voltage to any great degree.

Regulator Circuits

This section discusses some of the possible methods for using the Si7660 or Si7661 in constant-voltage output circuits over a given output current range. For low current inverter applications, the circuit shown in Figure 22 can be used. The output impedance of the circuit can be as low as 5 Ω with regulation up to approximately 20 mA. Note that if converters are paralleled on the output of this circuit, they should be synchronized to minimize output voltage fluctuations and output noise.

Another regulator application uses the Si7660 or Si7661 in a positive voltage regulator. Conventional three terminal voltage regulators have a voltage drop of greater than 1 volt between the input and output when operating with fairly heavy load currents. The circuit given in Figure 23 uses an Si7660 or Si7661 voltage converter to double the voltage which is then regulated by the op-amp and FET. This configuration allows regulation without the voltage drop as long as the input voltage does not drop below the Zener voltage plus the product of I_D times $r_{DS(on)}$.

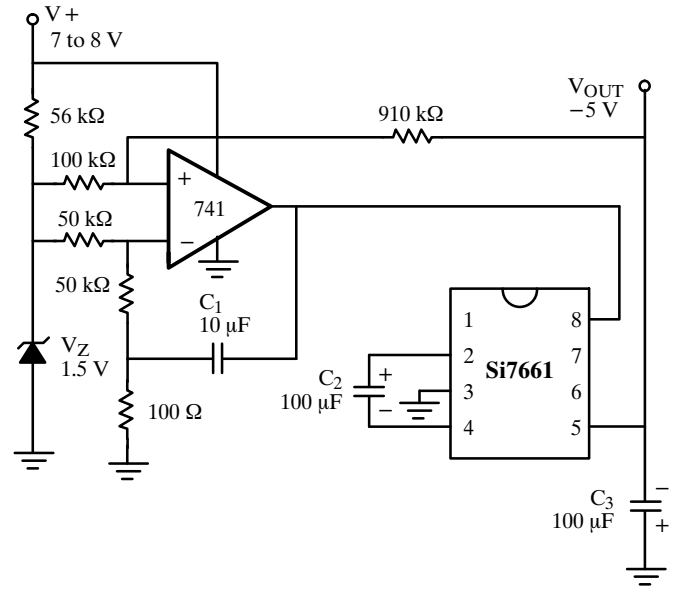


Figure 22. Low Current Inverting Regulator Circuit

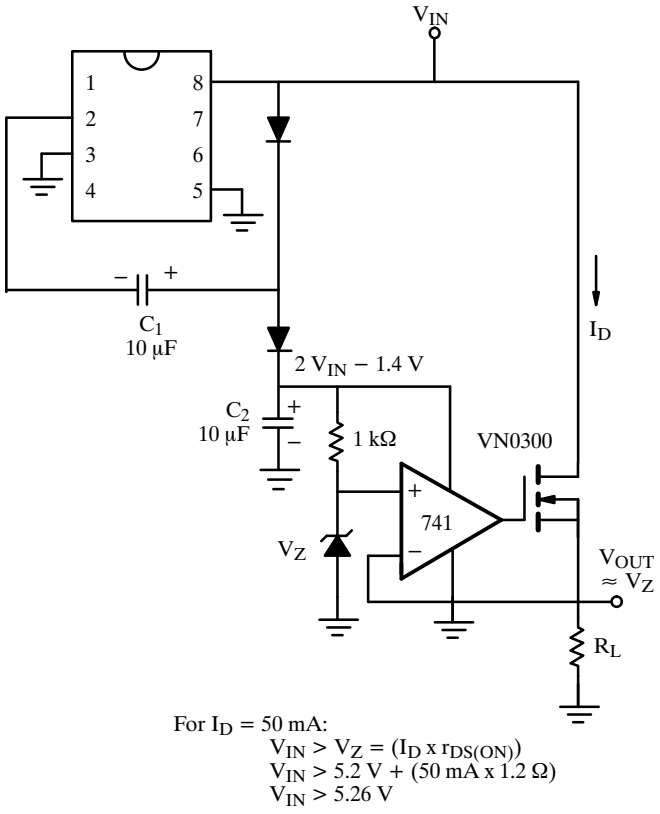


Figure 23. Schematic Diagram of the Positive Regulator Circuit

Therefore, as long as the input voltage does not drop below 5.26 V, the input is guaranteed to be regulated as close to the Zener voltage as can be attained by the common mode offset voltage of the op-amp. By selecting the correct Zener diode, this circuit can supply more than 100 mA and can be adjusted for varying voltage outputs up to the input voltage limit of the voltage converter.

Conclusion

The Si7660 and Si7661 are inexpensive alternatives to full negative supplies in many different low cost applications. Although they are designed for generation of negative voltages, many different voltage levels can be generated with a few additional parts. The examples given here are only a few of the many possible applications that could utilize the benefits of reduced board space and cost that the Si7660 and Si7661 provide.